

FIG.1A

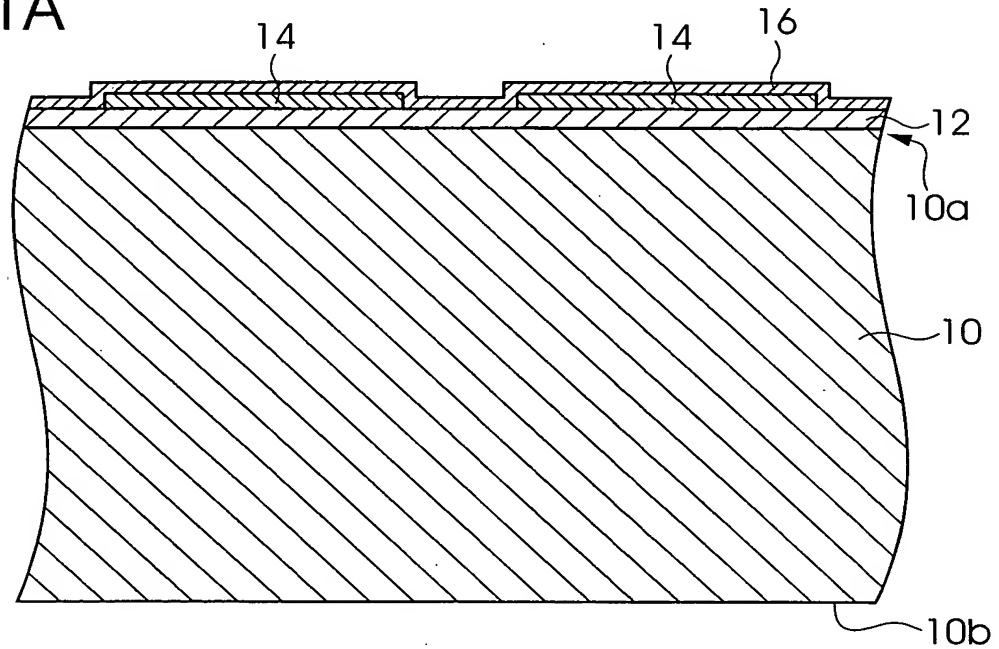


FIG.1B

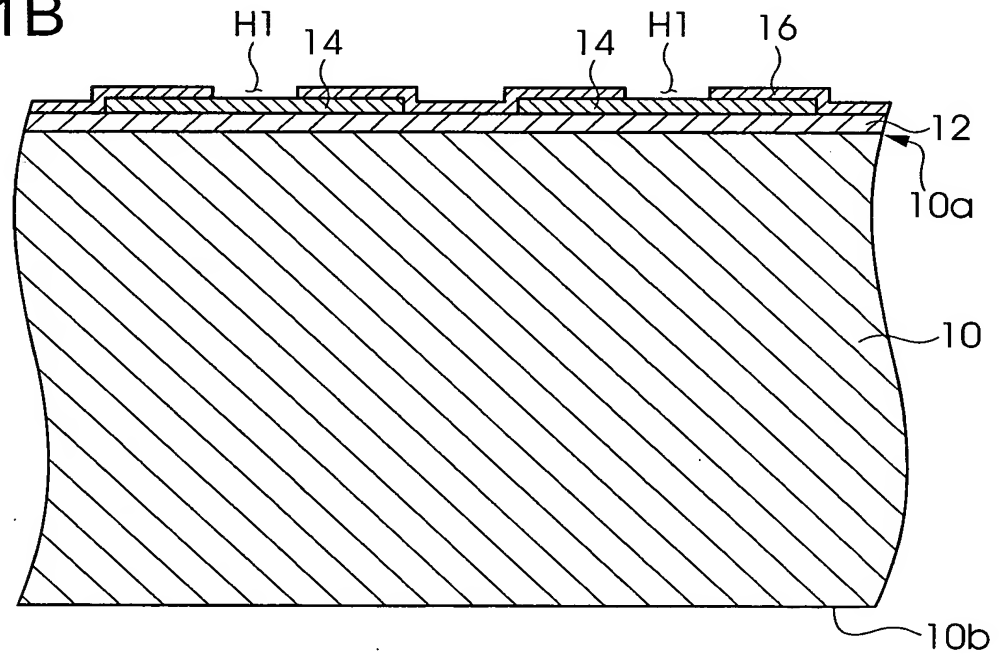


FIG.2A

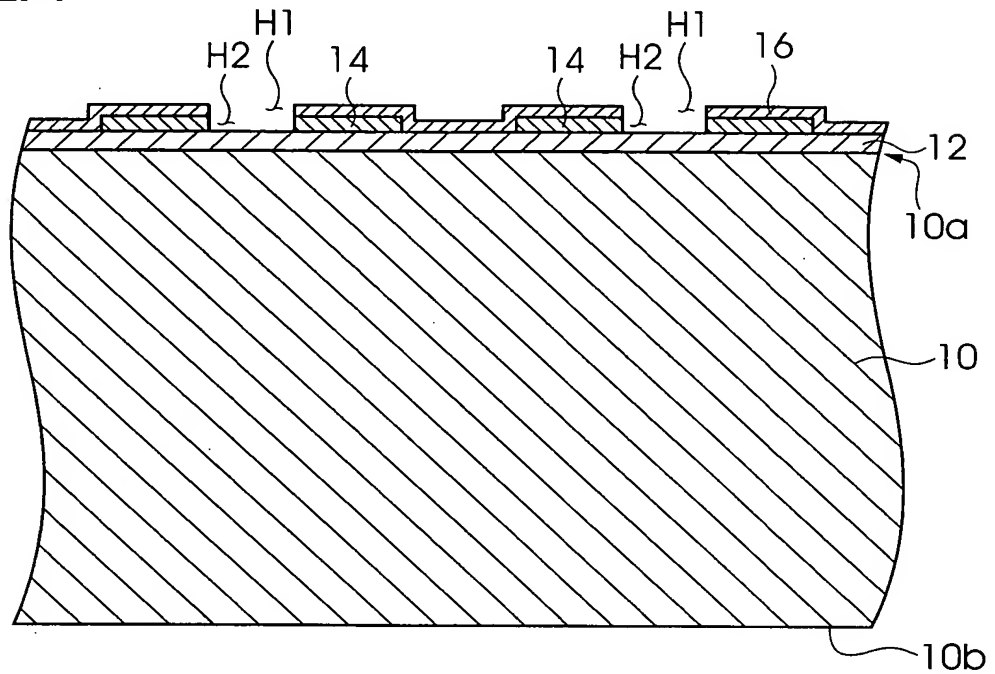


FIG.2B

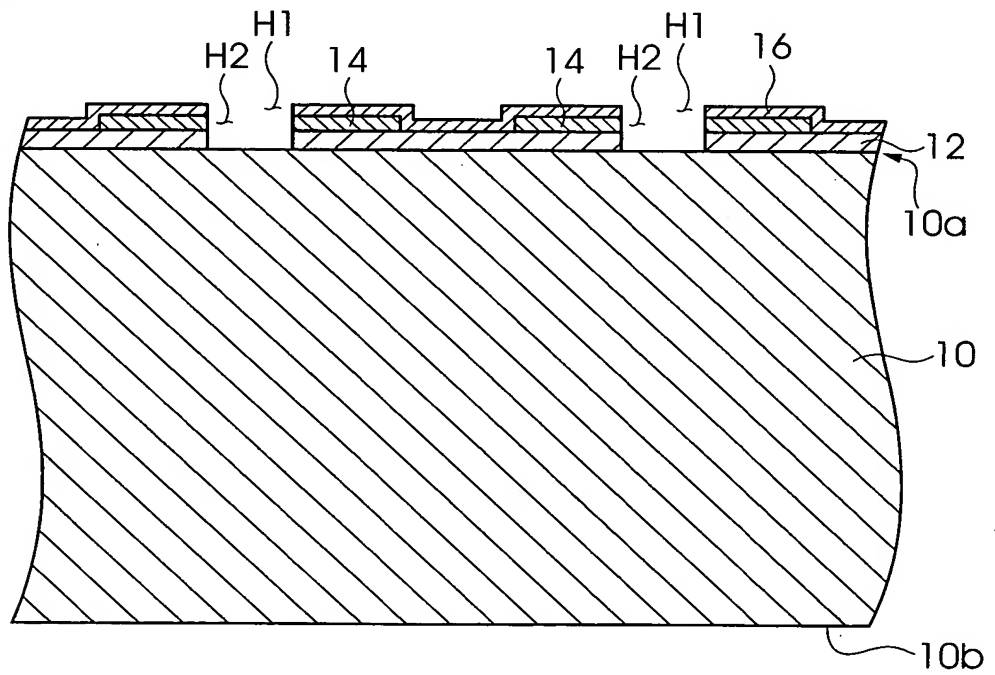


FIG.3A

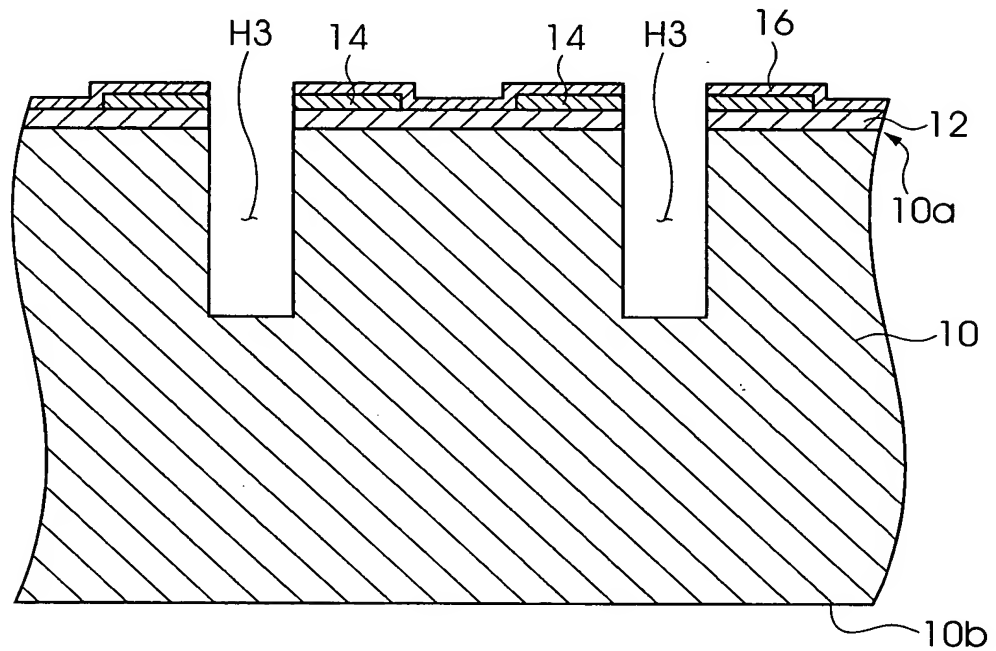


FIG.3B

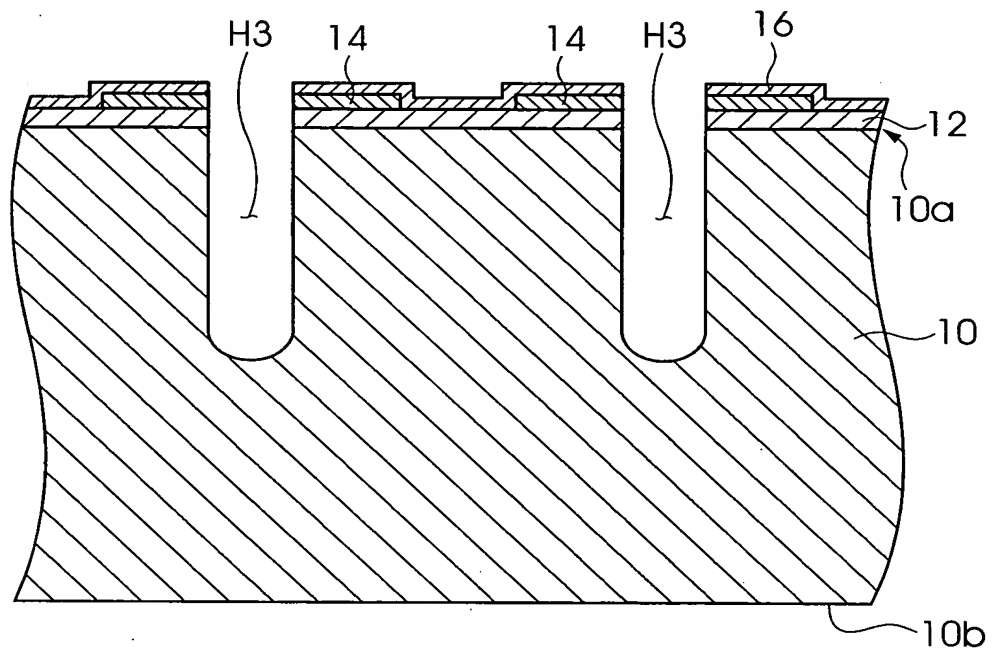


FIG.4A

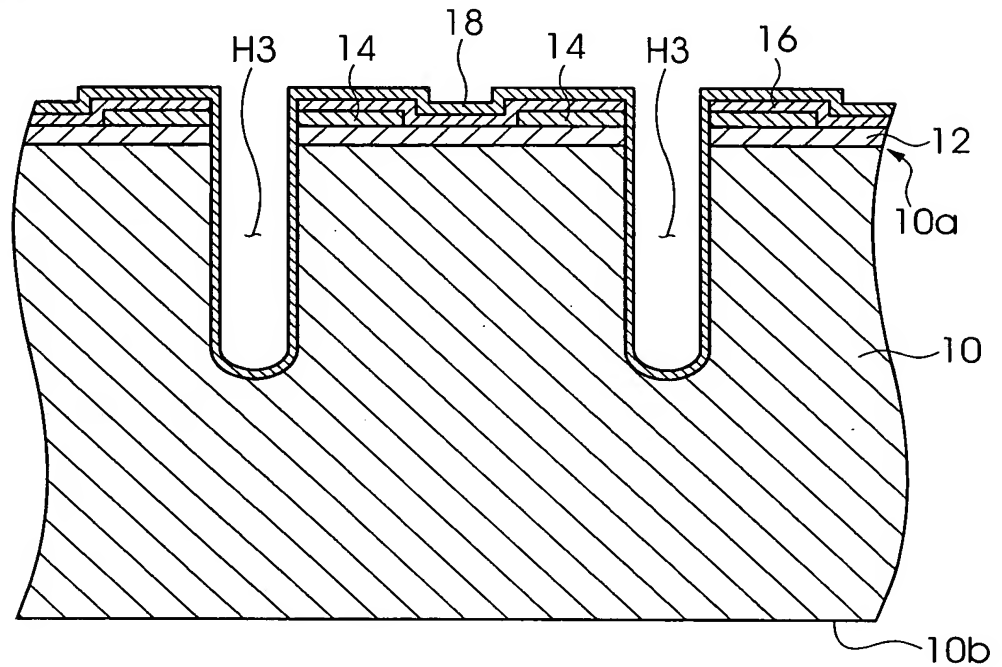
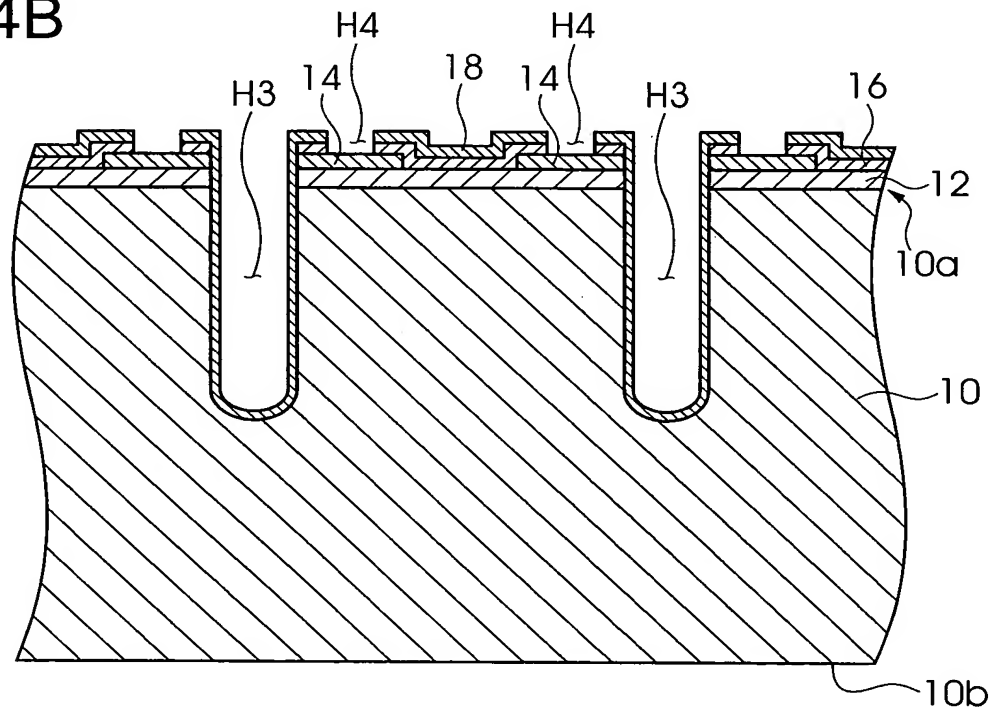


FIG.4B



This cross-sectional view shows a substrate 10 with a patterned layer 20 on its top surface. The patterned layer 20 consists of a series of rectangular blocks. Between these blocks, there are vertical vias 18 that extend from the top surface of the substrate 10 down to its bottom surface. The vias 18 are filled with a material, likely an insulator, and are surrounded by the patterned layer 20.

Figure 1C is a cross-sectional view of a semiconductor device. It shows a substrate 10 with a gate stack 18 and a gate electrode 20. The gate stack 18 is formed on the substrate 10, and the gate electrode 20 is formed on top of the gate stack 18. The gate electrode 20 is divided into segments by insulating spacers.

FIG.6

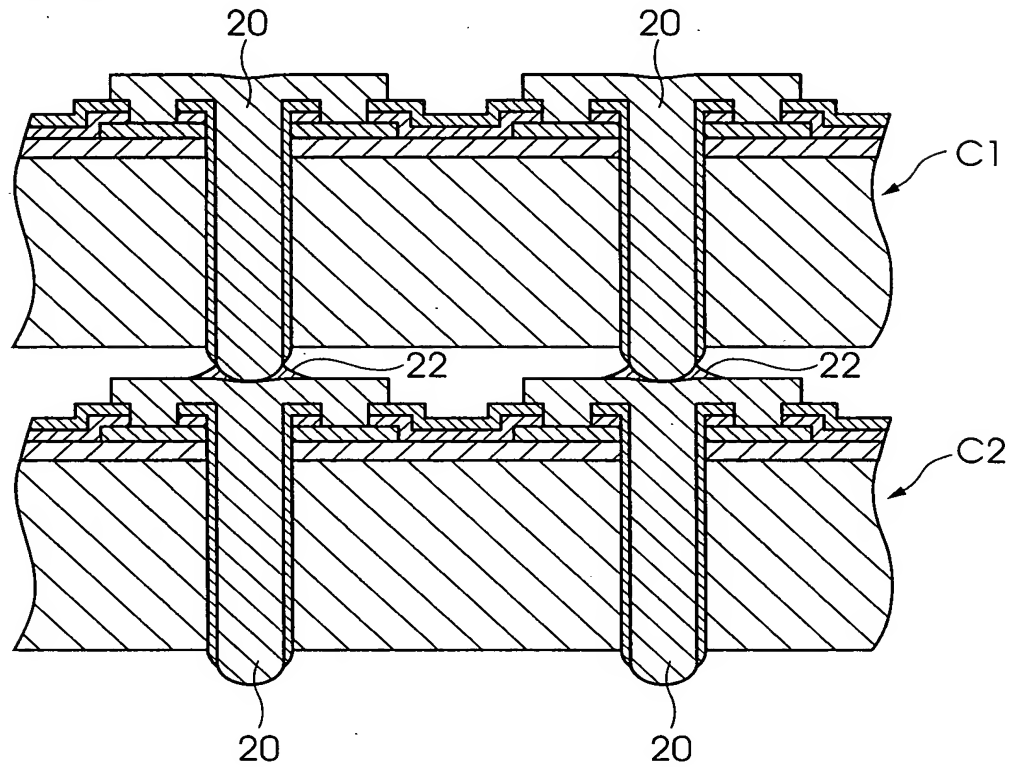


FIG.7A

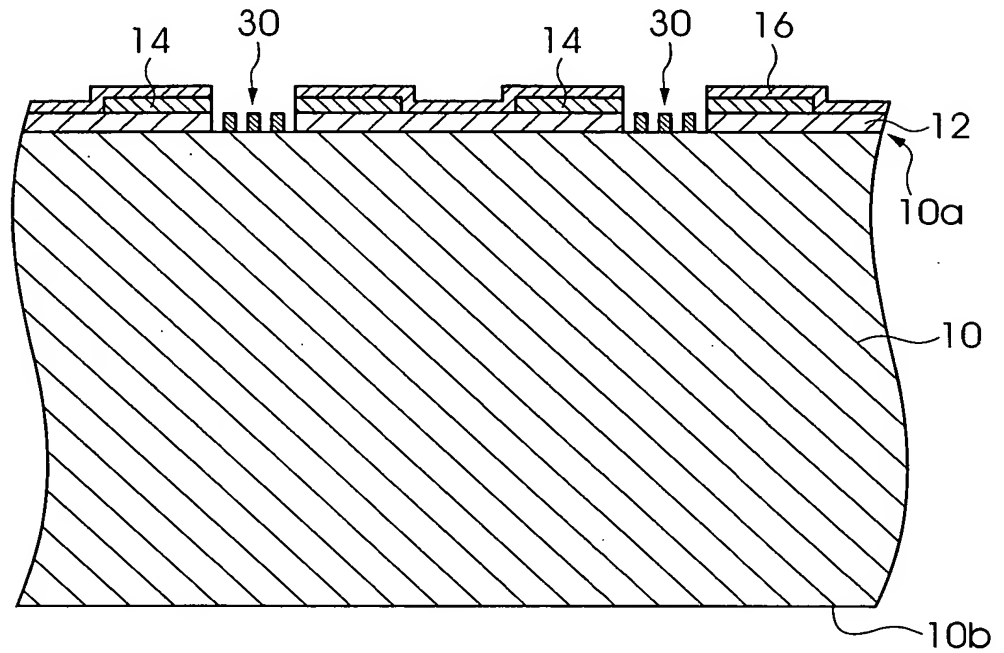


FIG.7B

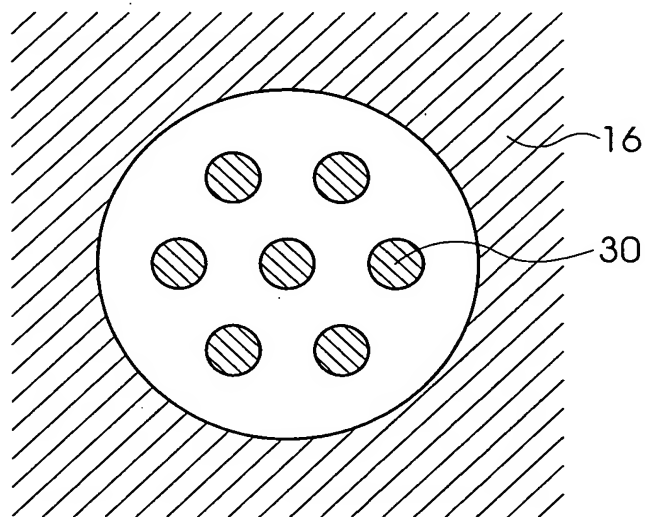


FIG.8A

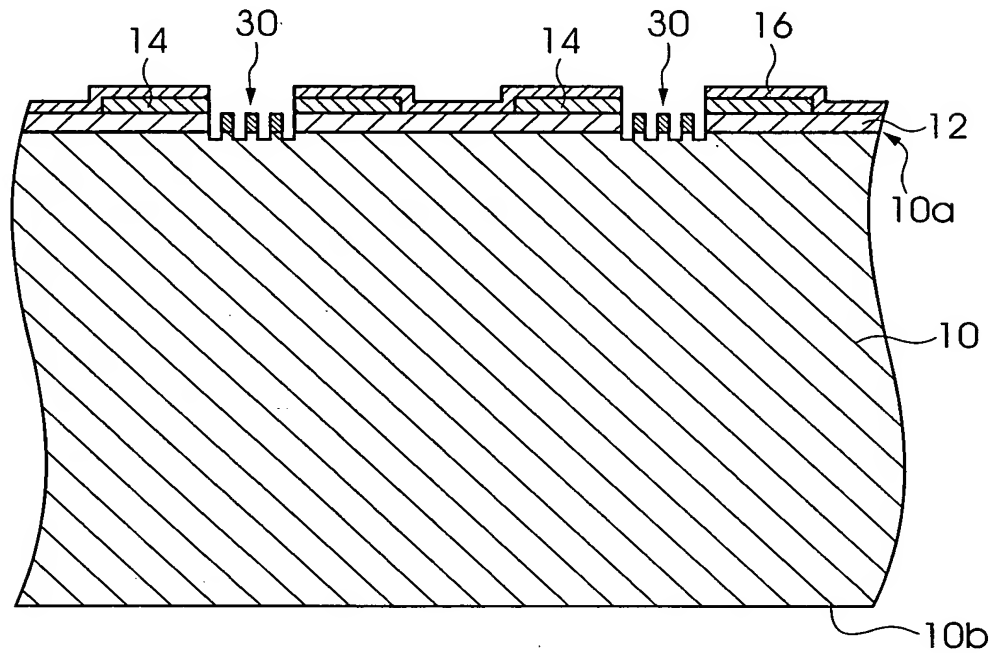


FIG.8B

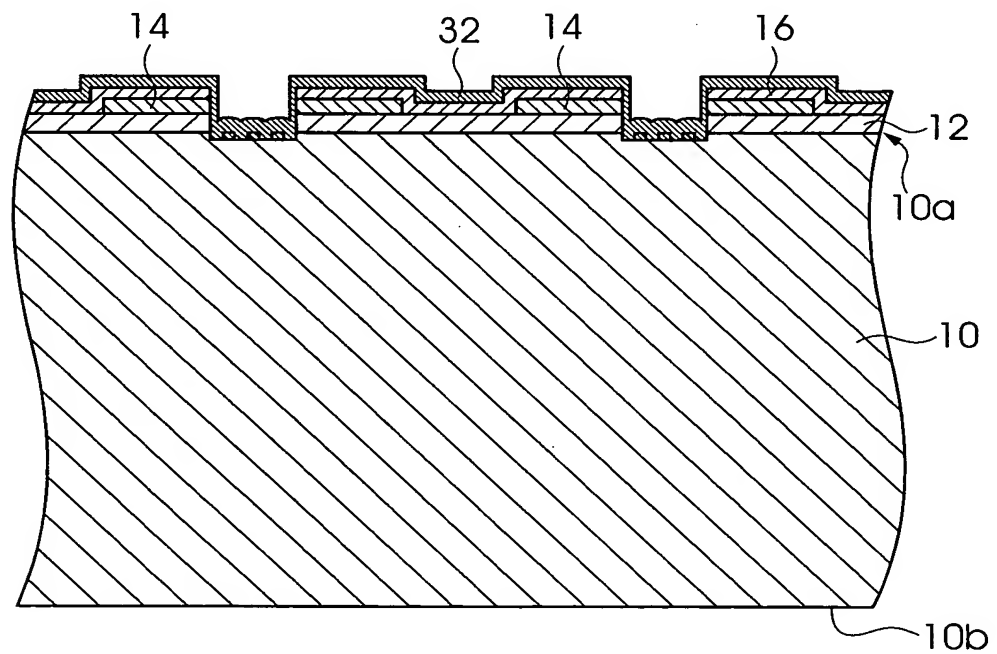




FIG.9A

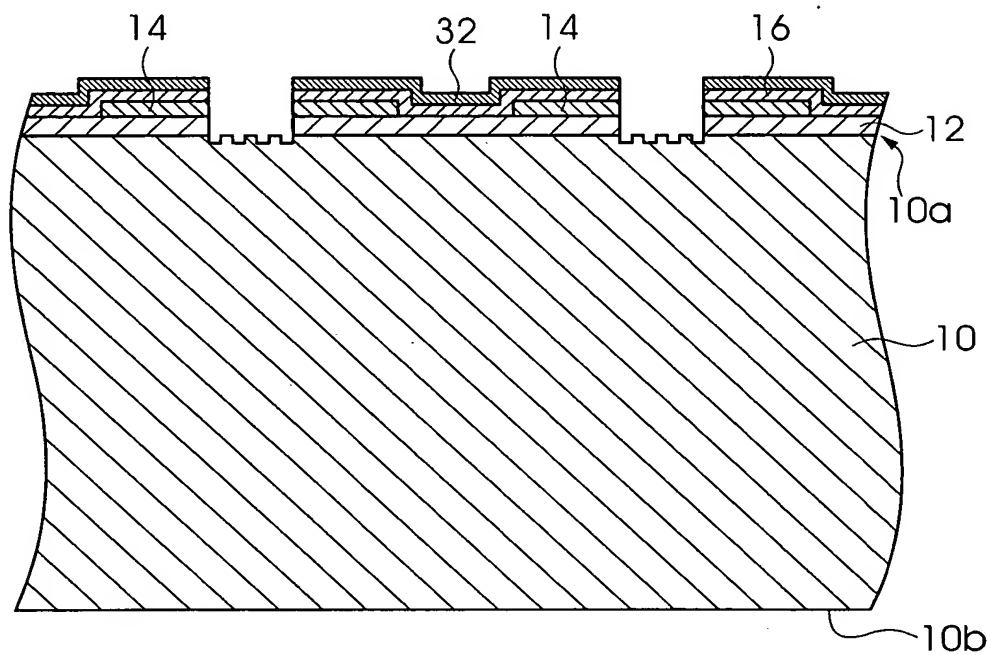
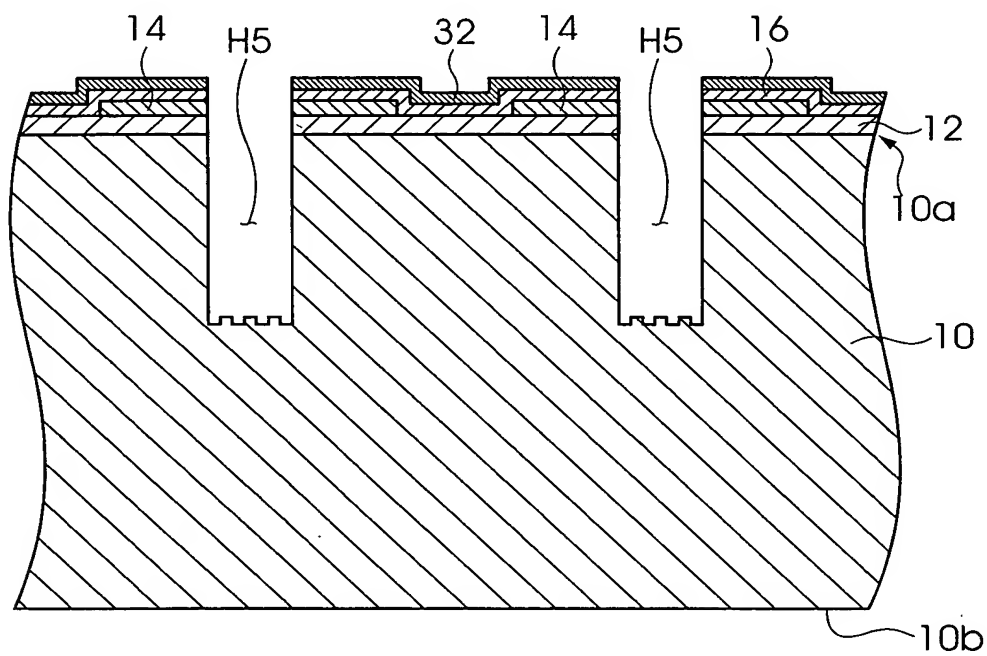


FIG.9B



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FIG.10A

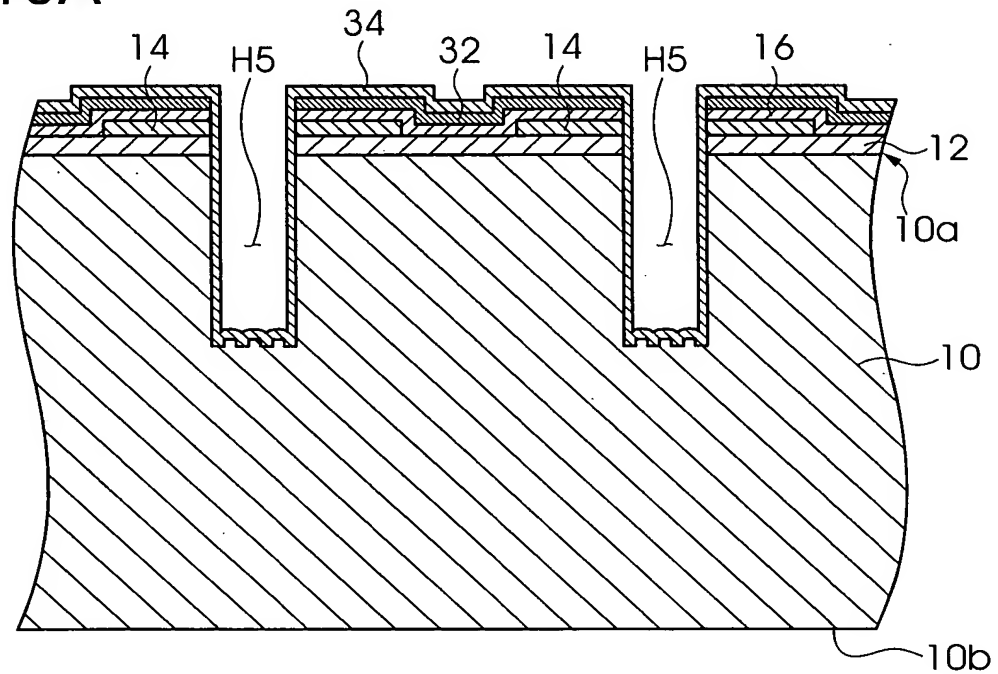
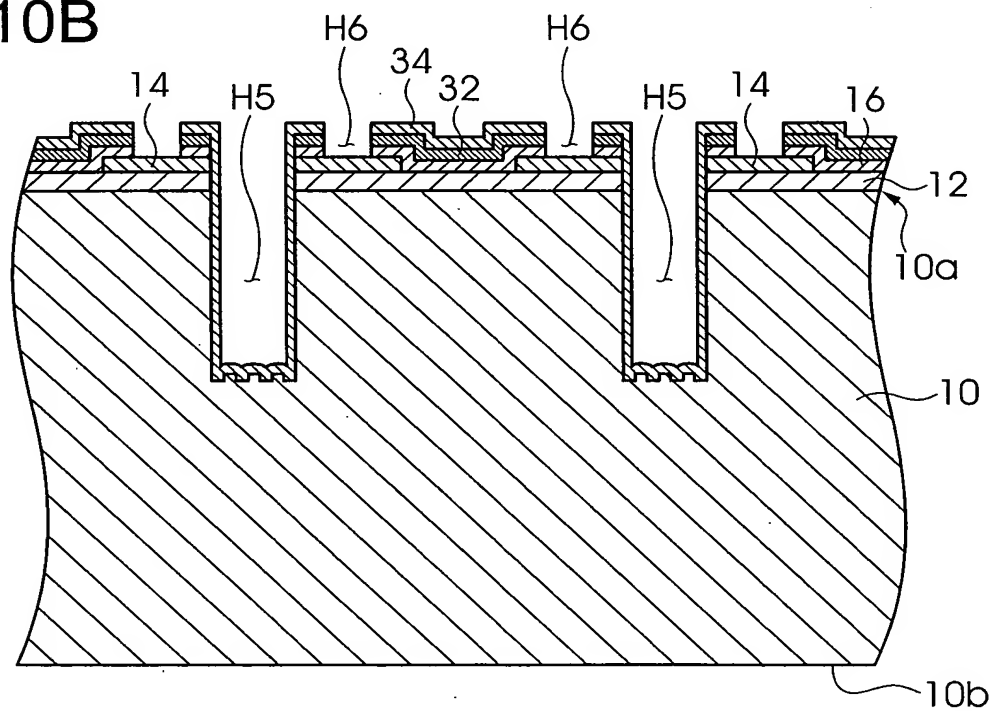


FIG.10B



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FIG.11A

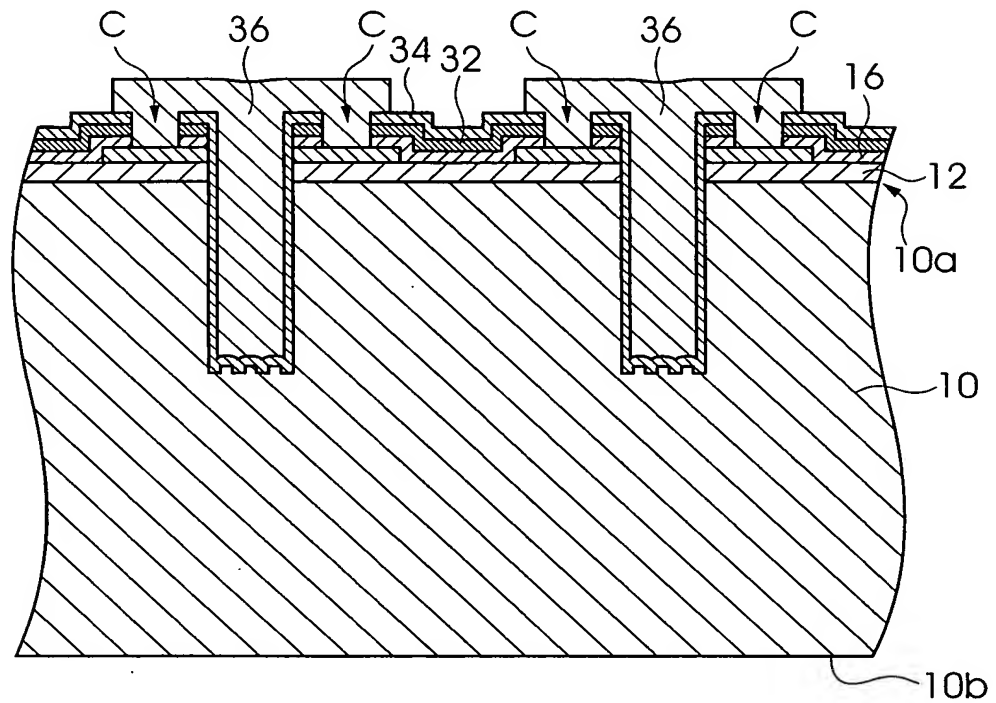


FIG.11B

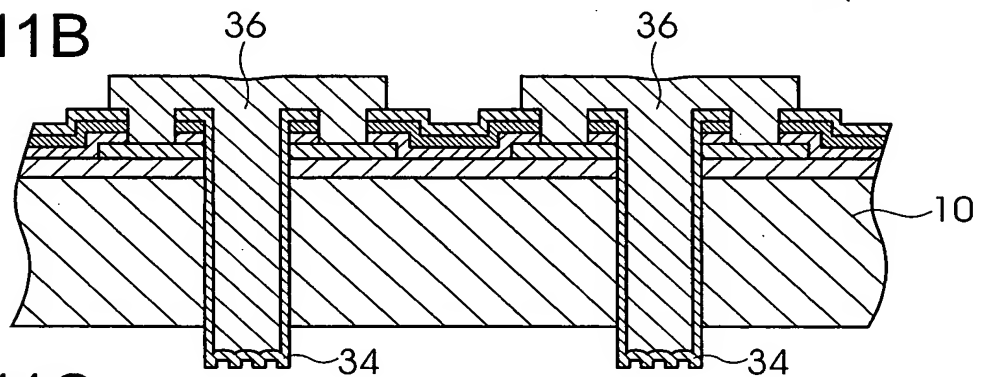


FIG.11C

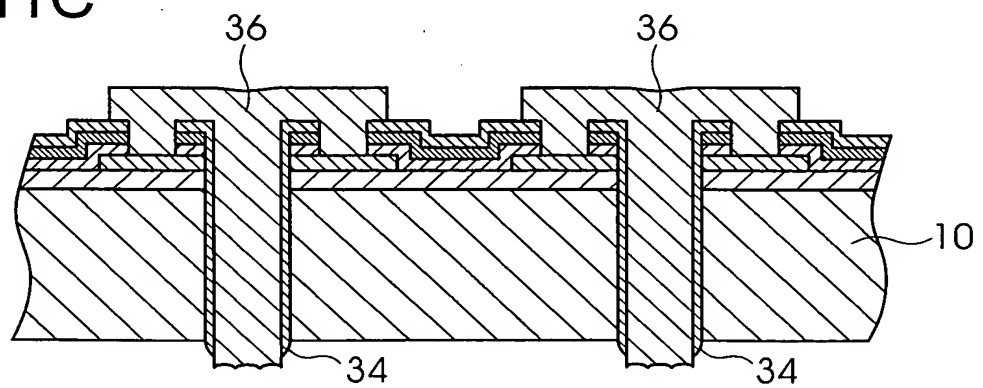
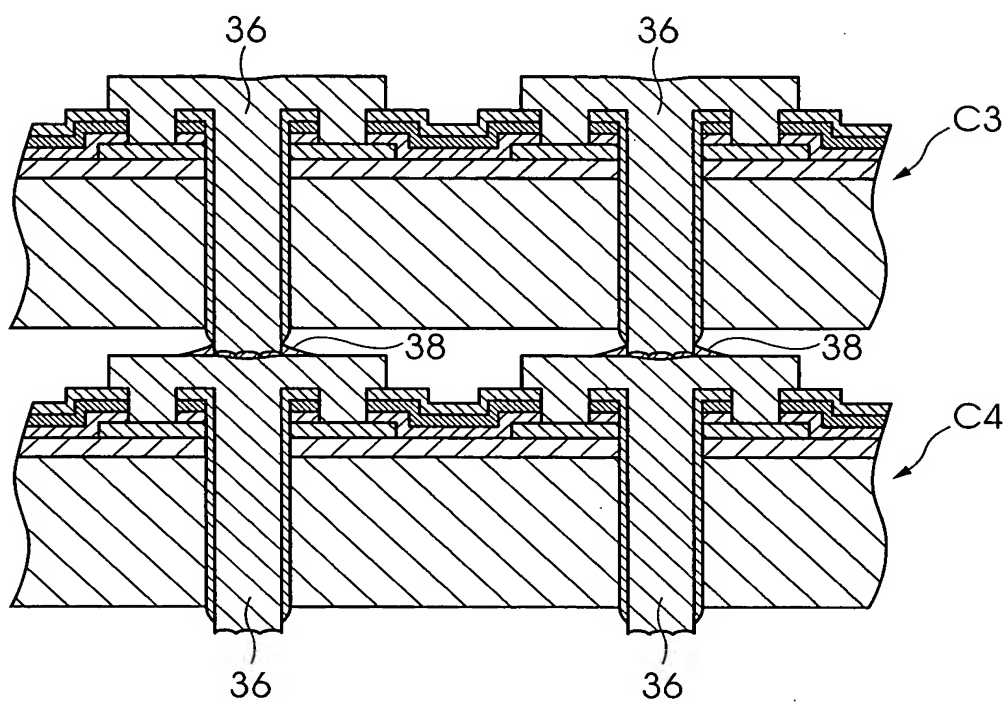


FIG.12



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FIG.13A

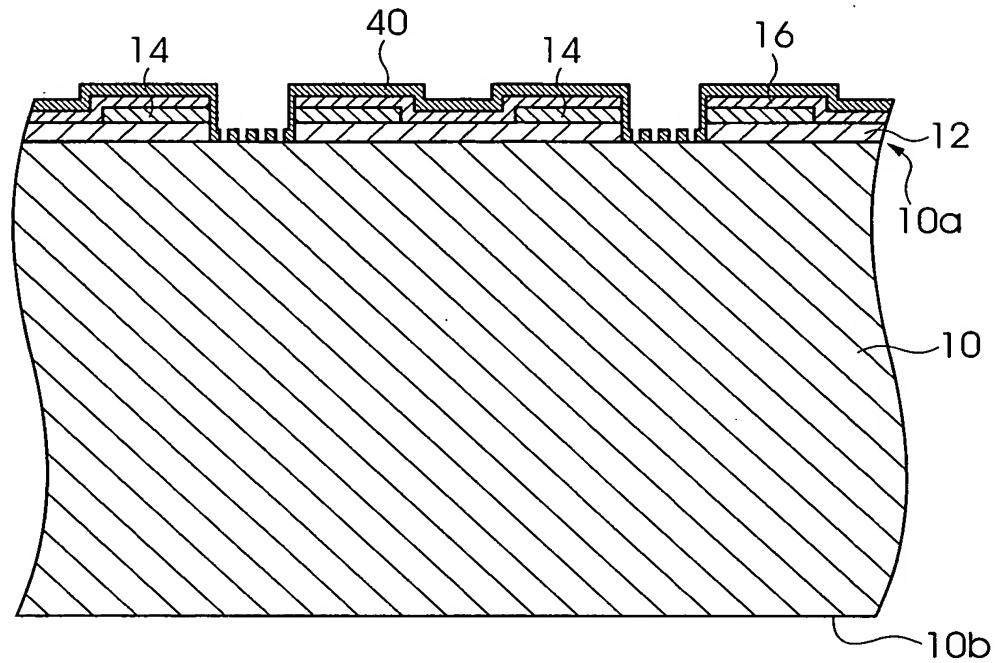
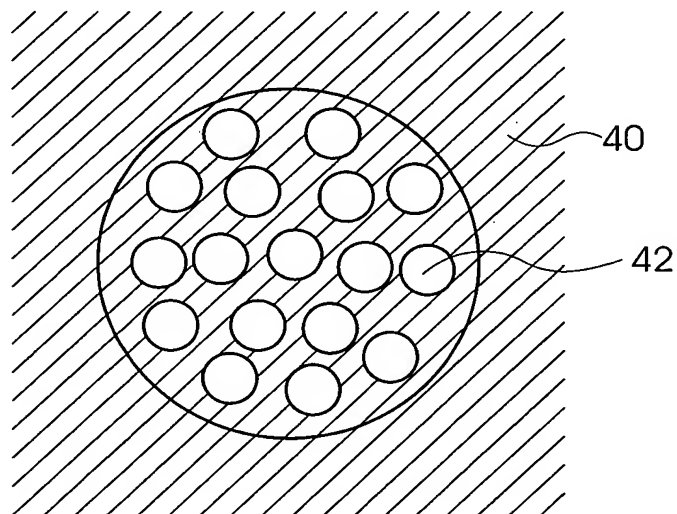


FIG.13B



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FIG.14A

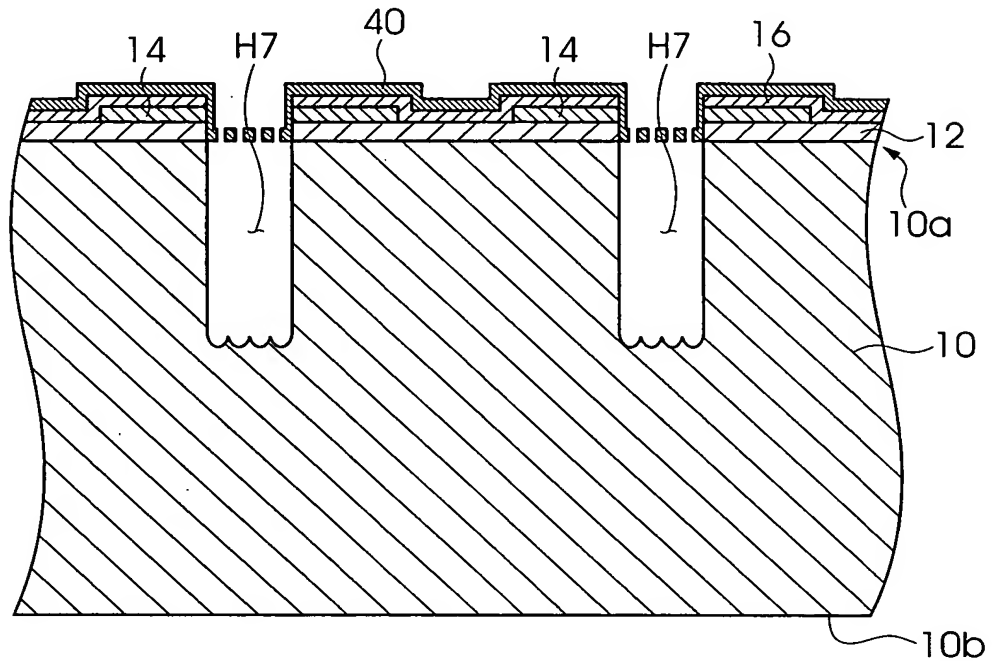
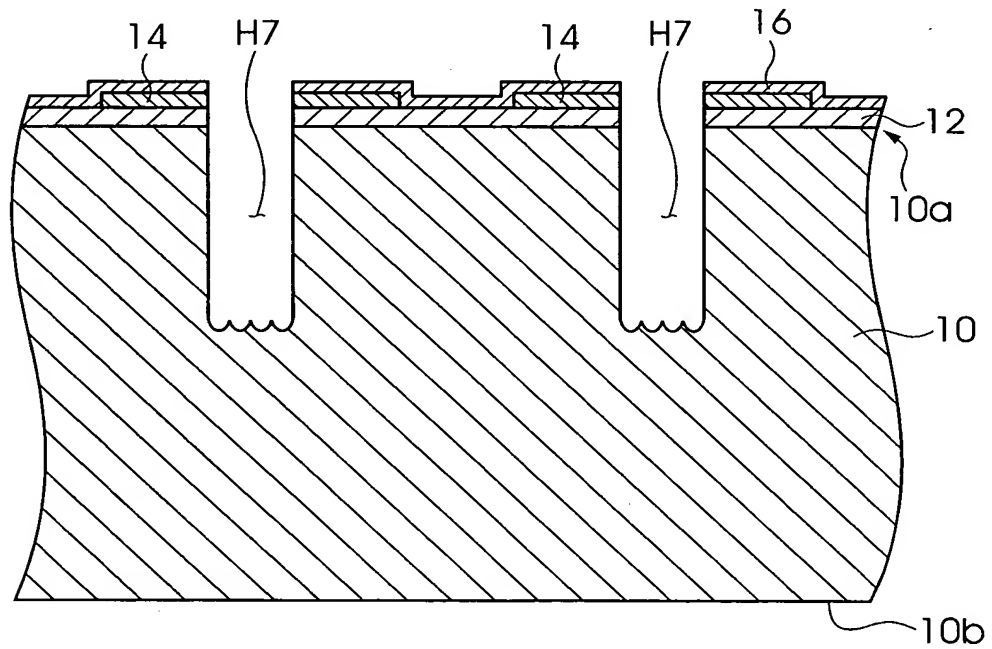


FIG.14B



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FIG.15A

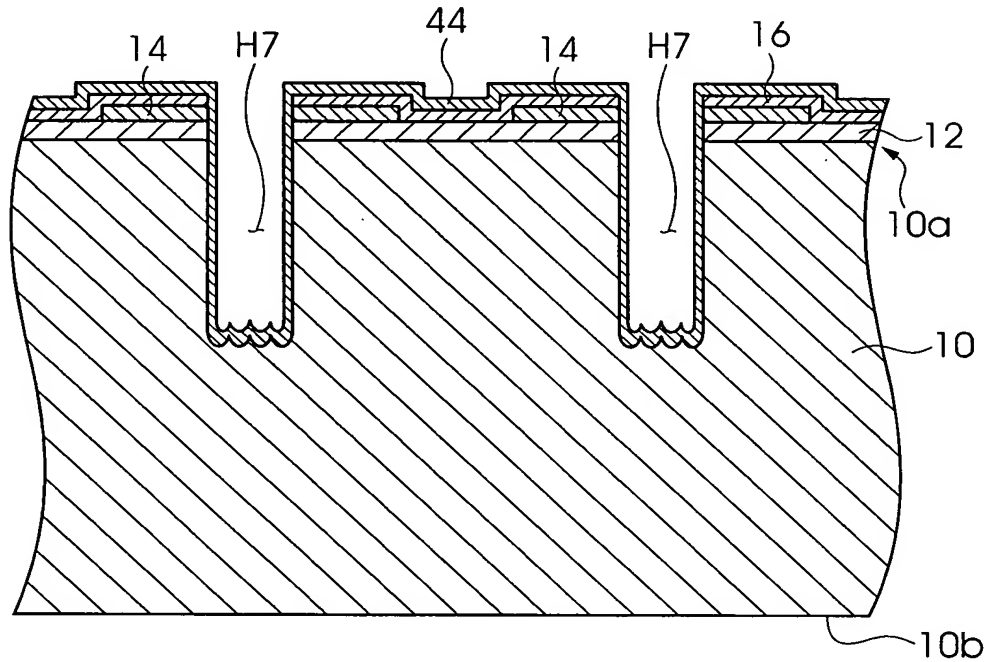


FIG.15B

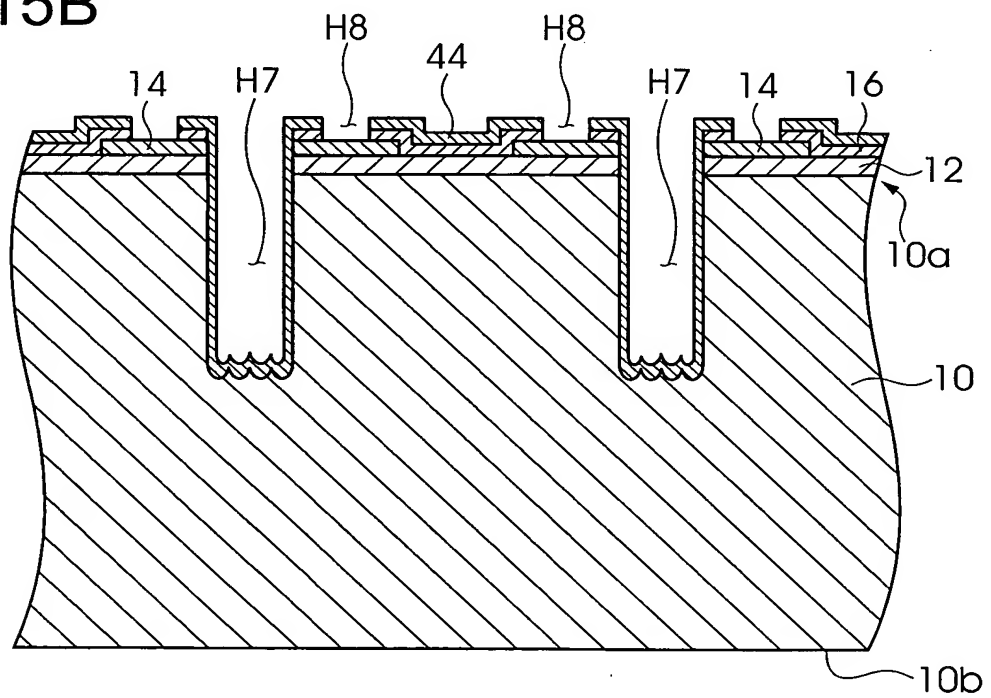


FIG.16A

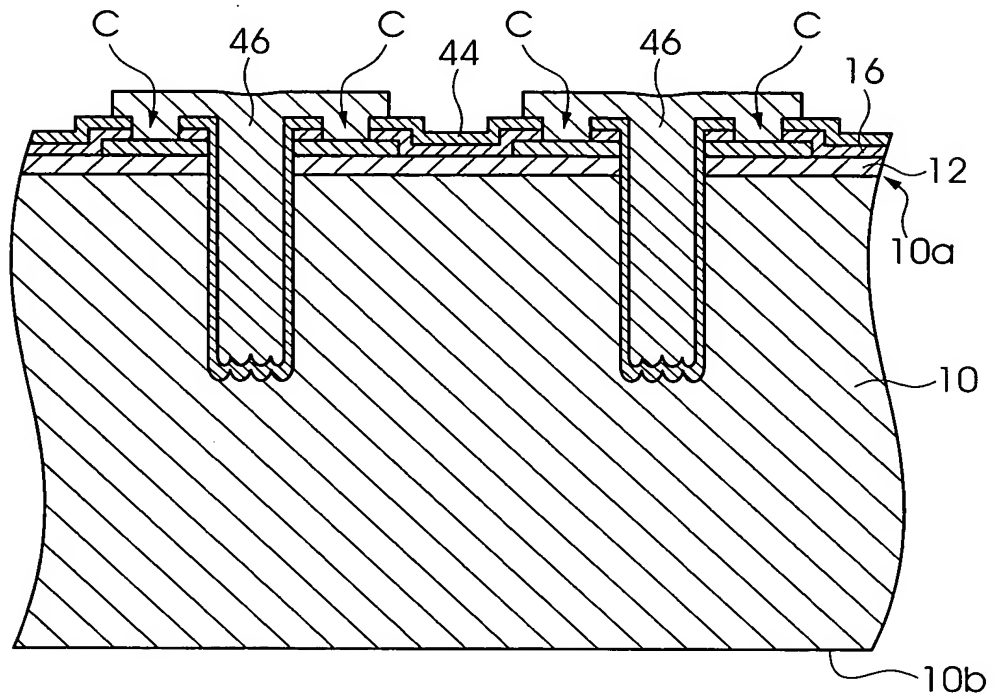


FIG.16B

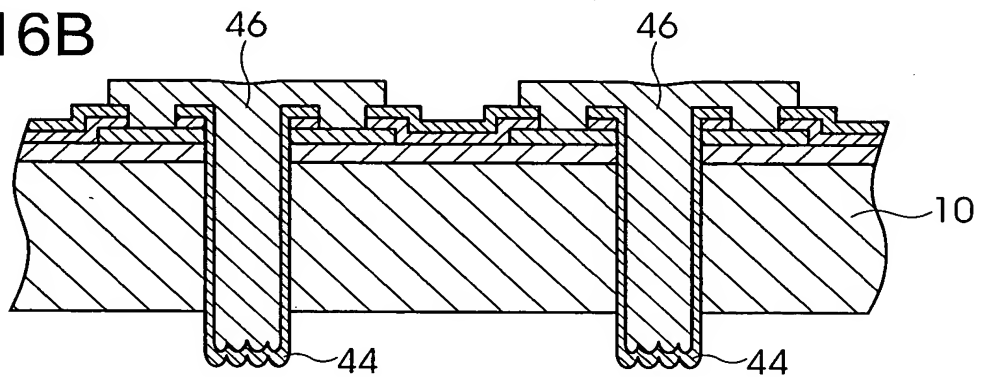
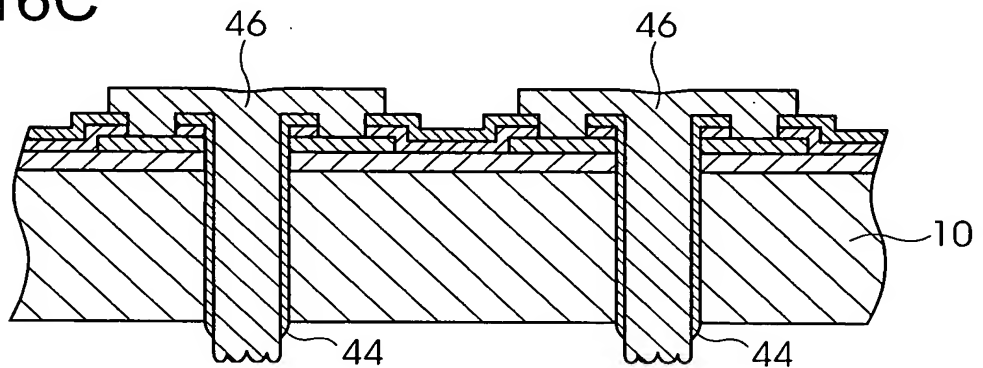


FIG.16C





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FIG.17

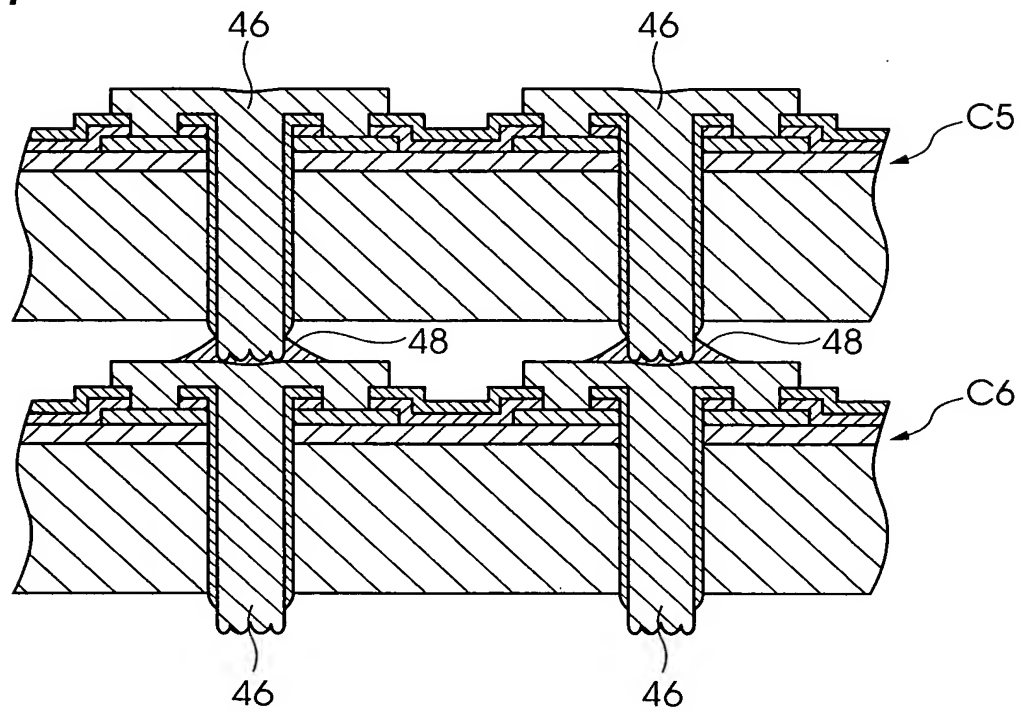


FIG.18

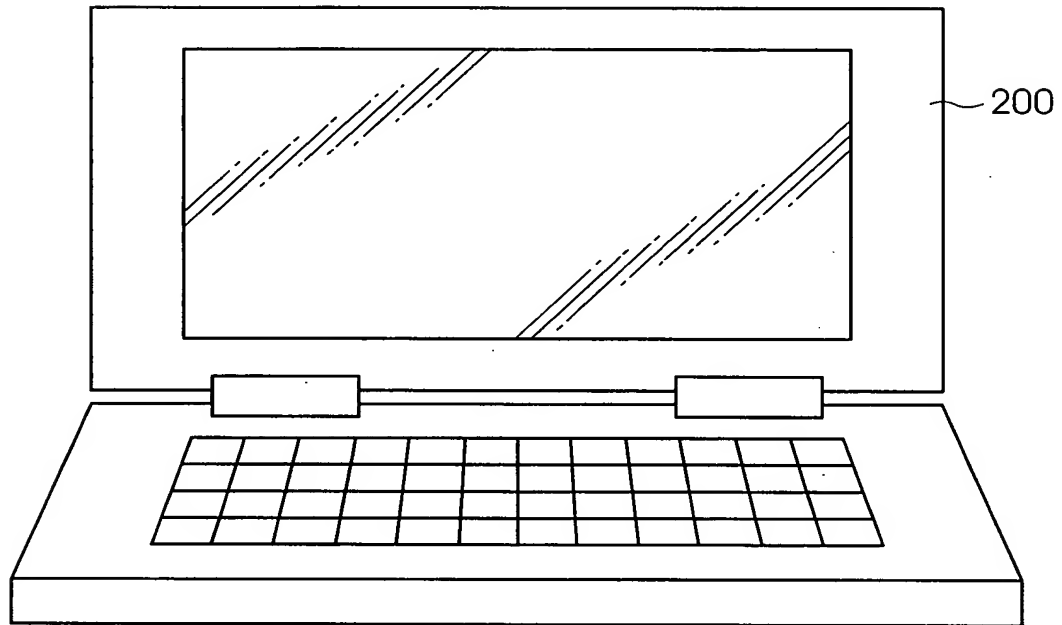


FIG.19

